VLSI Course Content:35-40hours

Course Outline

MOS Transistor Theory

- Introduction
- Ideal I-V Characterstics
- C-V Characterstics
- Nonideal I-V Effects
- DC Transfer Characterstics
- Switch -level RC Dealay Models

CMOS Processing Technology

- Only Briefing

Circuit Performance Estimation

- Delay Estimation
- Logical Effort and Transistor Sizing
- Power Dissipation
- Interconnect
- Design Margin

Combinational Circuit Design

- Introduction

- Circuit Famalies
- Comparison of Circuit Families

Sequential Circuit Design

- Sequencing Static Circuits
- Circuit Designs of Latches and Flip Flops
- Static Sequencing Element Theory
- Synchronizers

Datapath Subsystems

- Addition and Substraction
- One/Zero Detectors
- Comparators
- Synchronous Counter
- Boolean Logical Operations
- Coding
- Parity
- Multiplication
- Division

Design Methodology and Tools

- Platform Based Design
- Design Flows
- Design Economics

VHDL

- Bahaviour Modelling with Concurrent Signal Assignments
- Basic Constructs
- Bahavioural Modeling with Process Statements
- Finite State Machines
- Parameterized Blocks